REMARKS

Claims 1, 3, 5-9, 13-15 and 21-31 are pending in this application. By this Amendment, claims 2, 4, 10-12 and 16-20 are canceled, claims 1, 3, 5-9 and 13-15 are amended and claims 21-31 are newly added.

The Office Action rejects claims 2, 3, 6, 7, 10-14, 16 and 18 under 35 U.S.C. 112, first paragraph, as allegedly not being enabled by the disclosure.

First, with respect to the subject matter of claims 2, 3, 6 and 16, the Office Action contends that the specification does not disclose how correspondingly required regulated power at different required voltages is cost effectively derived and/or distributed. It appears there is a misunderstanding of this aspect of the invention. Contrary to the statement in the Office Action, this aspect of the invention is not about compensating for signal transmission delays that may result from more distantly placed memory arrays by operating such memories at higher voltages. Rather, this aspect of the invention intentionally drives each of the memory arrays with a different supply voltage so that the arrays will operate at different speeds but the signal paths of the memory arrays to the memory controller are made such that the data from the respective memories will arrive at the memory controller at approximately the same time. As is known in the art, there is a subsystem in a DRAM device called a "generator system" that generates all of the voltages and currents needed on the device for operation. One with ordinary skill in the art would know that the "generator system" on the memory device would generate the two different operating voltages for the two or more arrays. For these reasons, it is respectfully requested that this rejection be withdrawn.

Second, with respect to the subject matter of claims 10-14, the Office Action contends that these claims are not enabled because the specification does not describe how responses from the two memory arrays may be resolved from a common signal line. In response, there are many ways known in the art that the memory array responses can be resolved. The signal paths can be adjusted using well known design techniques such that it is known which memory array data will arrive at the memory controller before the other memory array data. Thus, *a priori* knowledge determined at the design stage is one method of resolving. If the two arrays have different wordline lengths (e.g., the embodiment of FIG. 5(a)), then it is quite easy to distinguish between the two memory array outputs because one will be a longer data packet than the other. For these reasons, it is respectfully requested that this rejection be withdrawn.

Third, with respect to the subject matter of claims 7 and 18, the Office Action contends that these claims are not enabled because the different circuit implementations for achieving the different sensing characteristics are allegedly not enabled by the specification. Claim 18 has been canceled. Claim 7 recites that one of the arrays is connected to and driven by a system supply voltage whereas the other array is connected to and driven by a ground potential. Sensing circuitry operated by a supply voltage (e.g., Vdd) is well known in the art. In addition, sensing circuitry driven by ground (such as for an NMOS array) is also well known in the art. This aspect of the invention concerns providing configuring one array to use the Vdd sensing scheme and the other array to use the ground sensing scheme in order to exploit the latency and cycle time differences of the two arrays in a desired manner. It is not necessary to disclose the details of the different sensing circuits that use these different sensing schemes because the circuits themselves are not part of the invention (or of the claims). This embodiment of the invention concerns the use of the dissimilar sensing schemes in the arrays. For these reasons, it is respectfully requested that this rejection be withdrawn.

The Office Action rejects claims 1-20 under 35 U.S.C. 112, second paragraph. In reply, the claims have been reviewed and amended where appropriate to comply with the definiteness requirements of the statute.

The Office Action rejects claims 1-20 under 35 U.S.C. 102(b) as being allegedly anticipated by, or in the alternative, under 35 U.S.C. 103(a) as being allegedly obvious over the cited reference to Benini et al. ("Benini").

Benini relates to automatic generation of a multi-bank memory architecture for embedded systems, and particularly to synthesizing a multi-bank memory architecture optimally fitted to an execution profile of an embedded application that runs on a given processor core. Benini further describes in his section 3.2 a partitioning tool that can, for a given number of words, produce different memory configurations using memories of different features in terms of "shapes of the memory (different aspect ratios), delays and power dissipation."

However, as recited in independent claims 1, 8 and 15, Benini does not teach or suggest the concept of providing at least first and second memory arrays that have dissimilar operating characteristics (but are addressed using a common addressing scheme) such that one of the arrays operates faster than the other of the arrays during a read or write operation.

As recited in claims 3 and 25, Benini does not teach or suggest at least two memory arrays that operate at different operating or supply voltages such that one of the arrays operates faster than the other, where the faster array is connected to a memory controller with a longer signal path than the signal path that connects the slower array to the memory controller.

As recited in claims 5 and 26, Benini does not teach or suggest at least two memory arrays, one of which has a shorter wordline length than the other, where the memory array having the shorter wordline length is connected to a memory controller by a signal path that is shorter than the length of the signal path that connects the memory array with the longer wordline length.

As recited in claims 7, and 27, Benini does not teach or suggest at least two memory arrays, one of which has sensing circuitry driven by a system supply voltage and the other of which has sensing circuitry driven by a ground potential such that one of the arrays has a faster cycle time than the other, but has a longer latency interval than the other. Further, as recited in claims 21 and 28, Benini does not teach or suggest that multi-byte information is read out from the arrays by reading a first byte from one array, followed by a second byte from the other array and followed by a third byte from the other array.

Benini does not teach or suggest at least two memory arrays: one of which has a refresh rate and refresh current that is greater than a refresh rate and refresh current of the other array (claims 22 and 29); one of which has more cells per bitline than the other array (claims 23 and 30) and one of which has at least two sub-arrays, each having the same number of cells per bitline (claims 24 and 31).

In sum, Benini fails to teach the concepts described in the independent as well as the dependent claims.

Based upon the foregoing, it is respectfully submitted that the present application is condition for allowance. Should the Examiner have any questions or comments, he is cordially invited to telephone the undersigned so that the present application may receive a prompt Notice of Allowance.

Submitted herewith is a check in the amount of $50 for the one additional dependent claim over and above the claims covered by the filing fee. No extension of time or other fees are believed to be due. However, Applicants hereby petition for any extension of time that may be necessary to maintain the pendency of this application. The Commissioner is hereby authorized

to charge payment of any additional fees required for the above-identified application or credit any overpayment to Deposit Account No. 05-0460.

Dated: March 27, 2006

Respectfully submitted by
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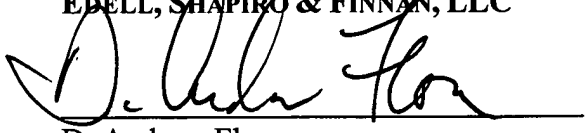
By: 
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